



# Simulation investigation of resolution enhancement techniques (RETs) in low k1 EUV

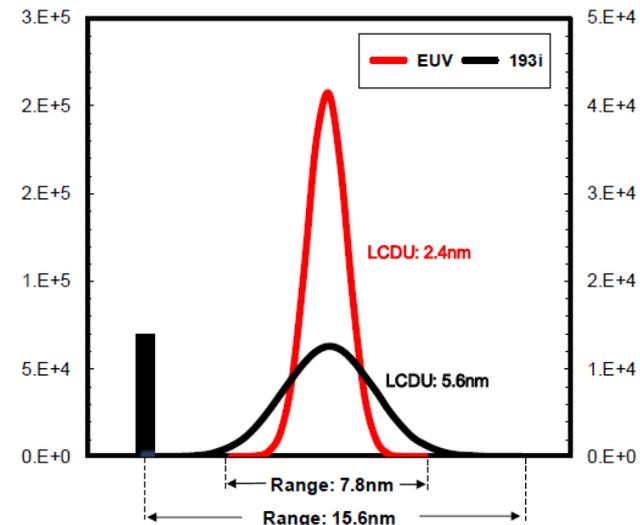
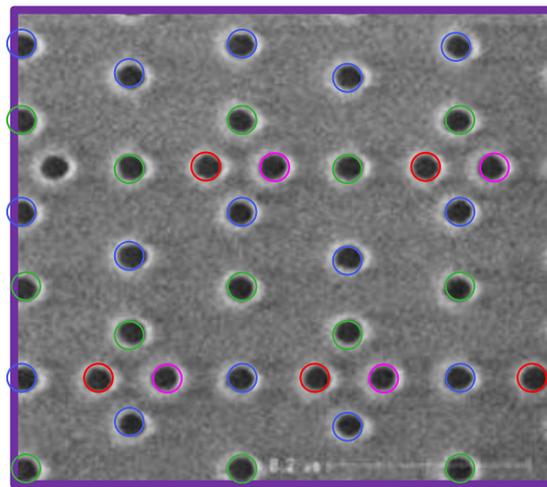
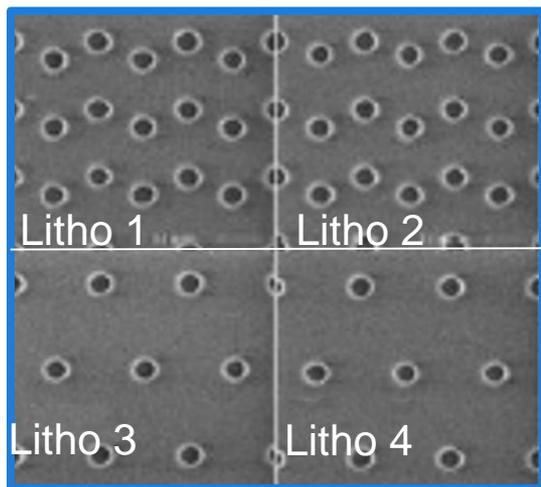
Boer Zhu, Wei-Min Gao

ASML

IWAPS 2020  
Chengdu, Sichuan, China  
05-06 November 2020

# EUV SP vs 193i MP: improve LCDU

Via with 193i multiple patterning (left) vs. EUV single-patterning (right)

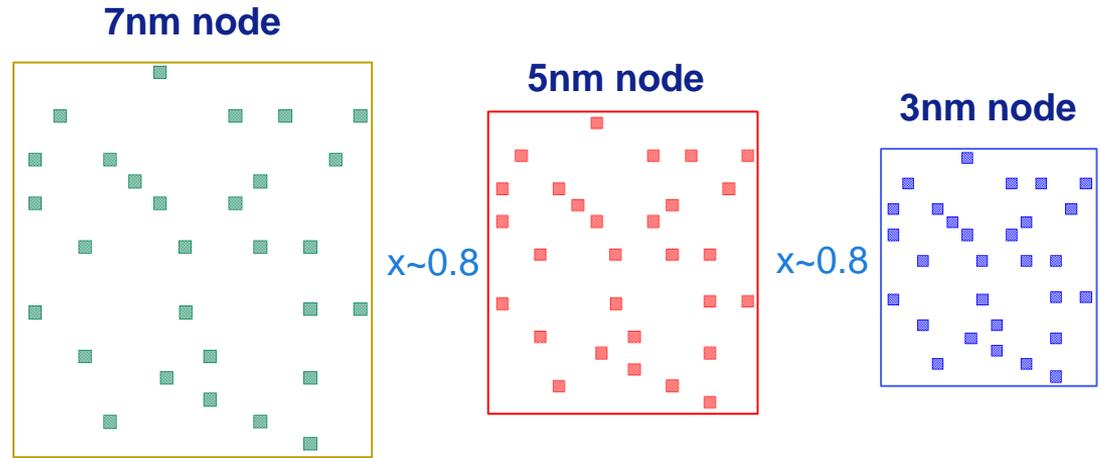
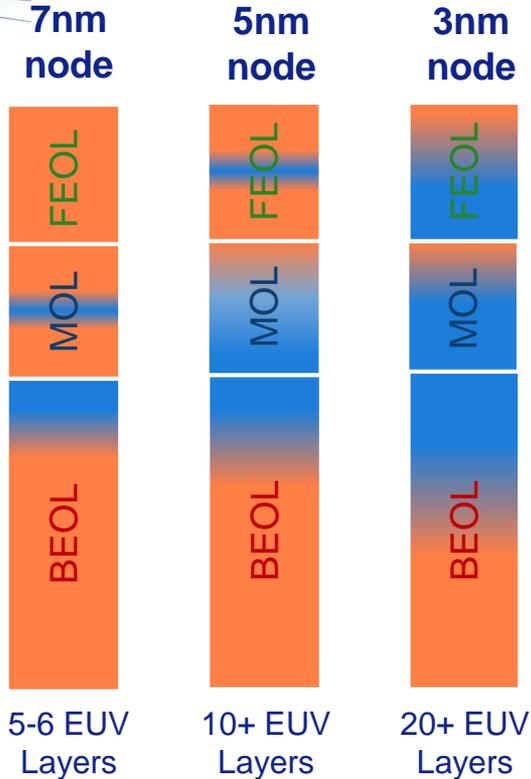


Local Critical Dimension Uniformity (LCDU) and process control of single patterning EUV (Red) vs. multiple-patterning 193i (black) showing 2-3X improvement.

As high volume production requirements had been satisfied by the EUV technology, we started the volume ramp of the enhanced 7nm technology with EUV insertion in 2019. Looking forward, the usage of EUV layers for 5nm technology node and beyond will continue to increase.”

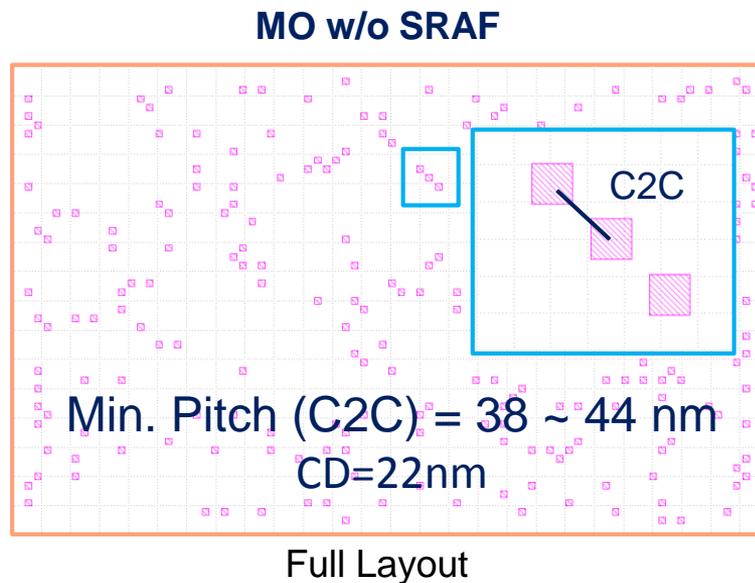
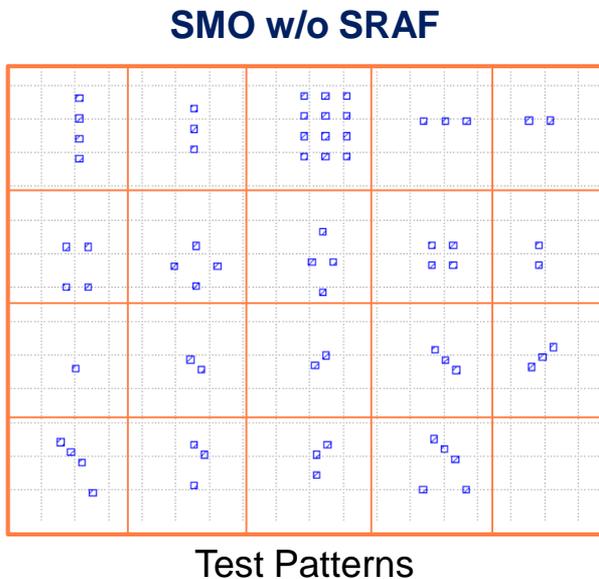
S.-Y. Wu (TSMC), “Key Technology Enablers of Innovations in the AI and 5G Era,” IEDM, San Francisco, 11 December 2019

# Trends of EUV layers #'s and Via pitches in Logic IC



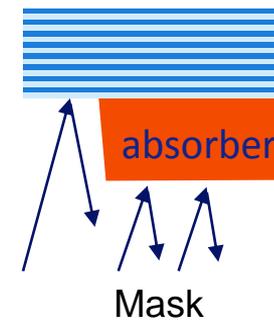
- Our studies indicate that Via pitches shrink by ~20% node to node
  - Current EUV SP could pattern vias pitch around 43 – 45nm.
  - How about EUV SP for pitch range from 38 – 44nm
  - EUV SP for Via layers is key to maintaining cost-effectiveness

# Layout, simulation method and nominal conditions

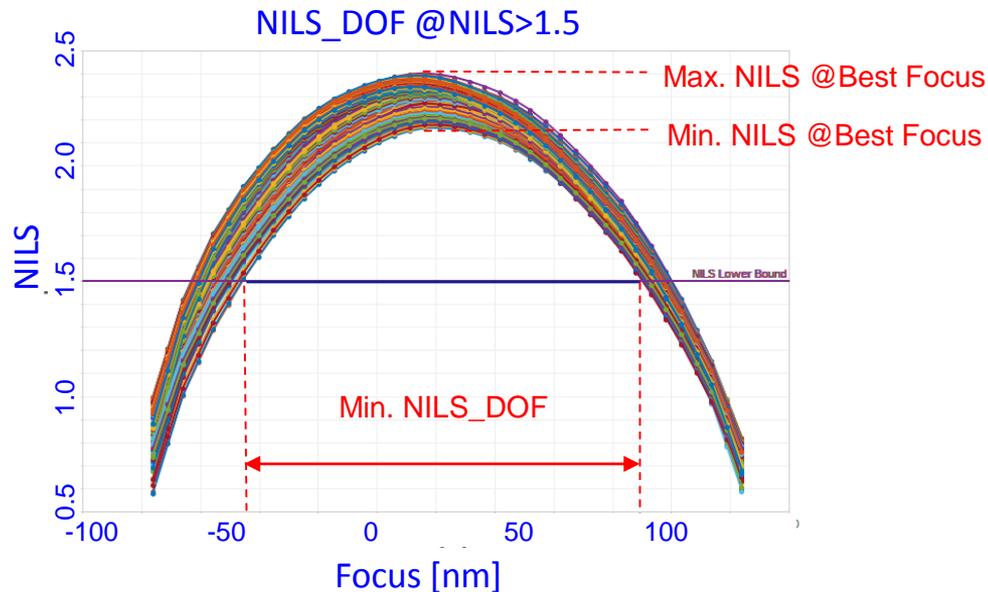
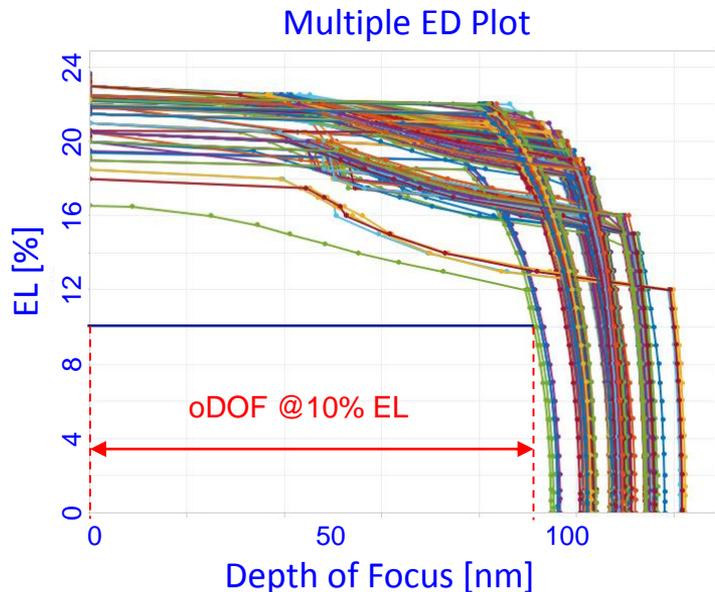


## The following conditions are used in simulations

- EUV Scanner: NXE3400X
- Mask: 40x Mo/Si multiple layer with a 55-nm thick Ta-based absorber
- Resist: CAR (30nm)
- Imaging: Dark-field mask with M3D and calibrated resist models



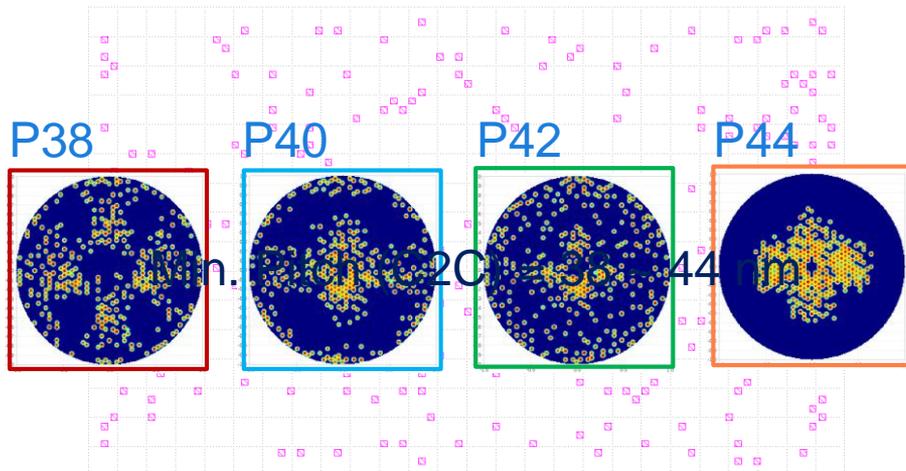
# Litho Metrics (oDOF, NILS, NILS\_DOE)



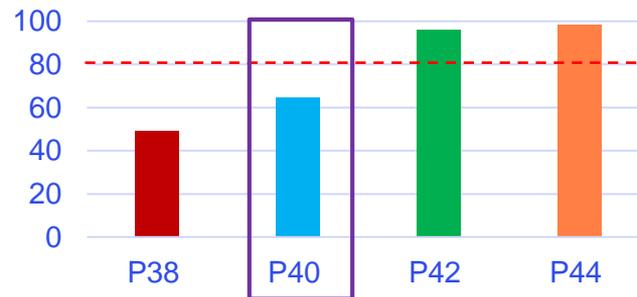
- **oDOF (Overlapped DOF) @10% EL** = minimum overlap of CD DOF for all 1000 cut lines
- **Min. NILS\_DOE** = minimum overlap of NILS\_DOE for all 1000 cut lines
- **Min./Max. NILS @Best Focus** = minimum/maximum NILS for all 1000 cut lines at Best Focus

# MO results of logic Via vs. min. Pitch (C2C)

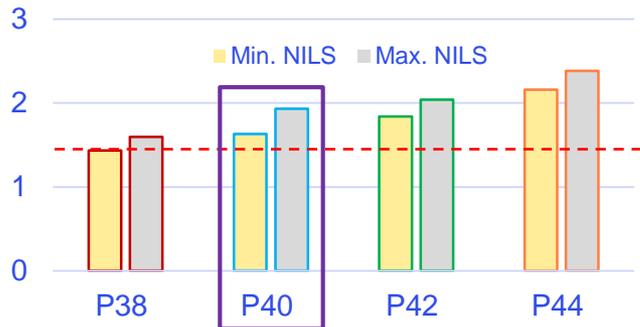
Based on Ta absorber



oDOF @ 10% EL



NILS @ Best Focus

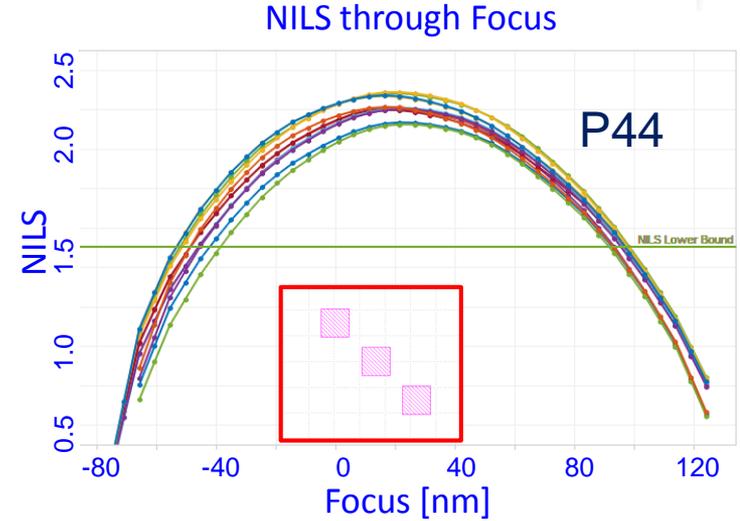
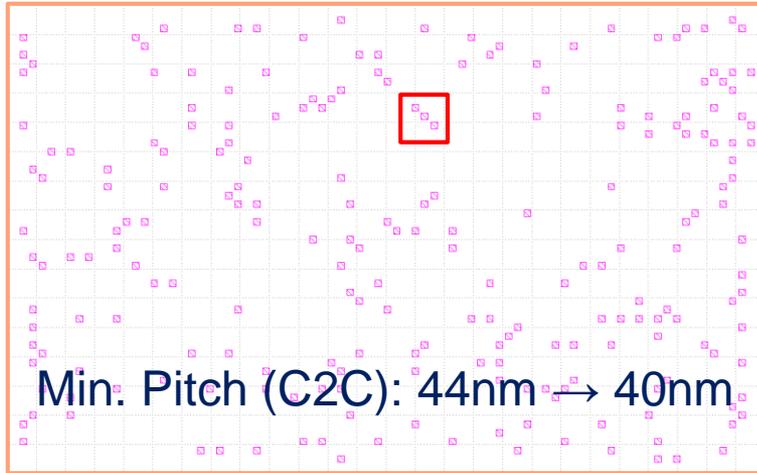


Min. Nils\_DOF @ Nils > 1.5



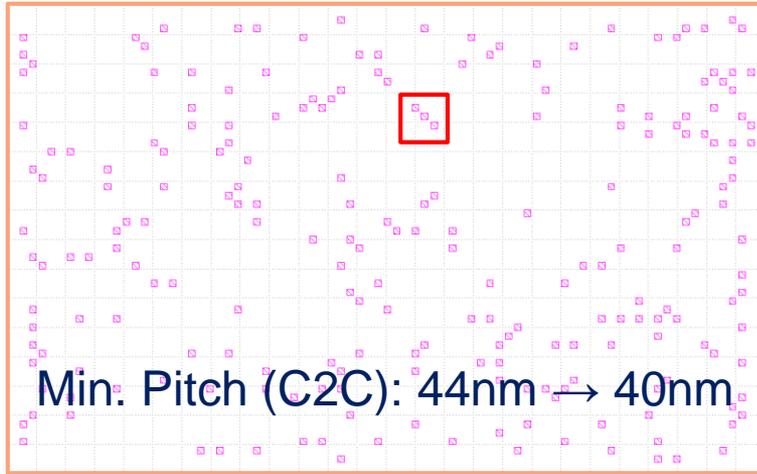
# Analysis between Min. Pitch 44nm and 40nm

Based on Ta absorber

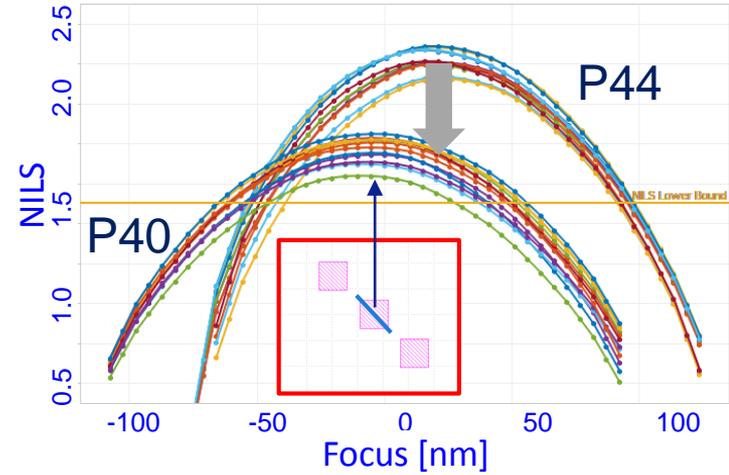


# Analysis between Min. Pitch 44nm and 40nm

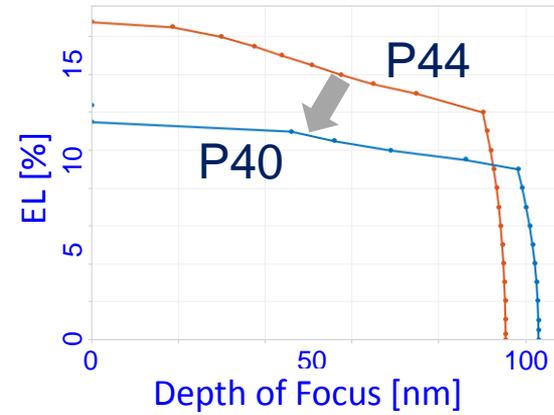
Based on Ta absorber



NILS through Focus

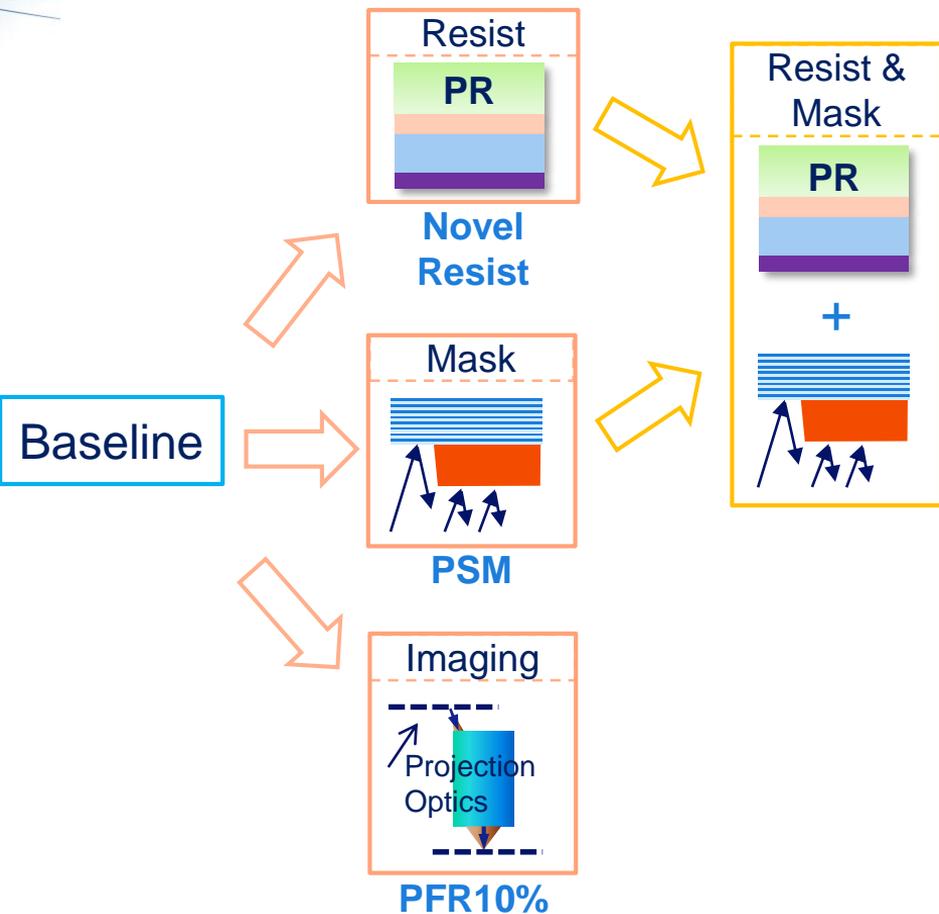


ED Plot

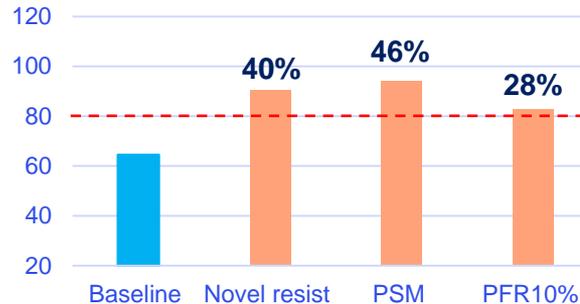


- NILS curve will dramatically decrease overall, when Min. Pitch shrunk.
- Diagonal cutline simultaneously limit the oDOF and NILS\_DOF.

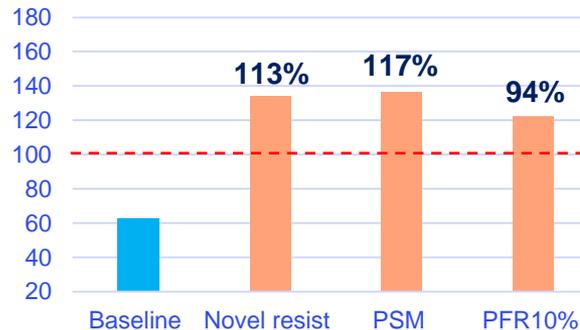
# MO results of RETs for logic Via with min. Pitch=40nm



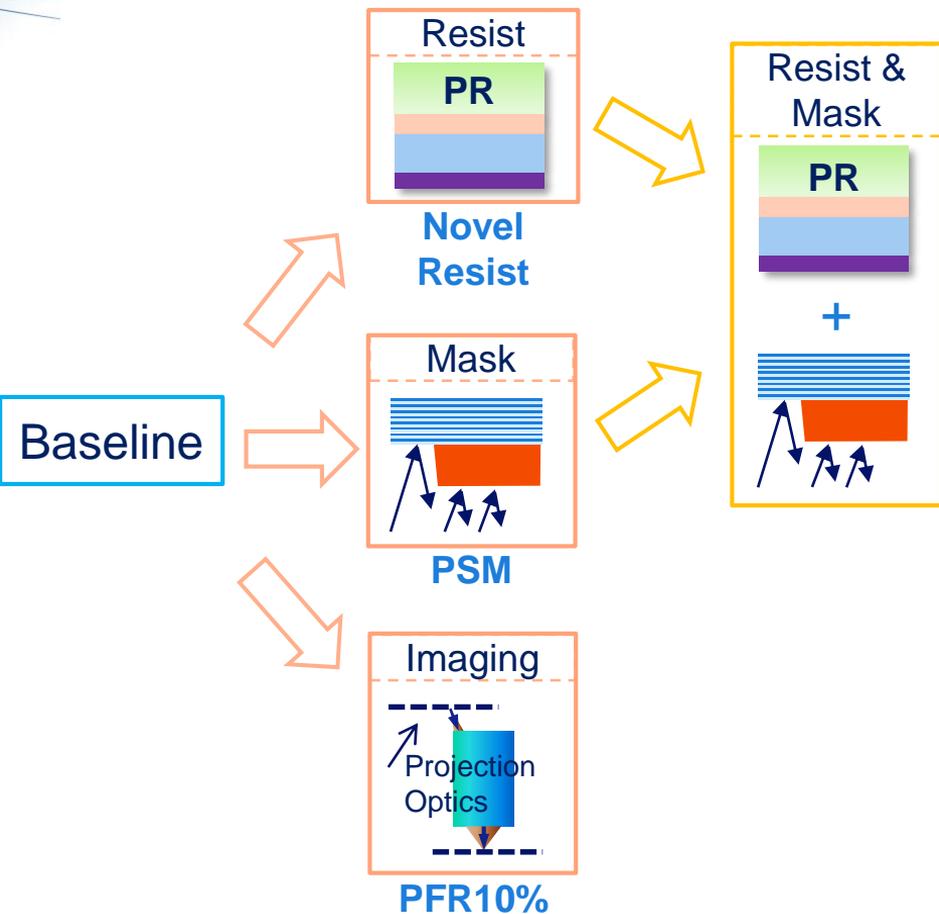
oDOF @10% EL



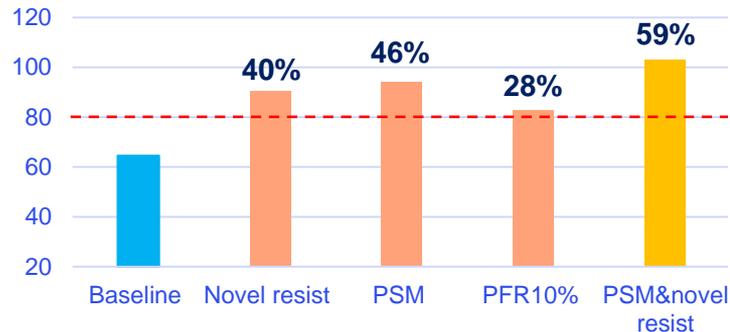
NILS\_DOE @NILS>1.5



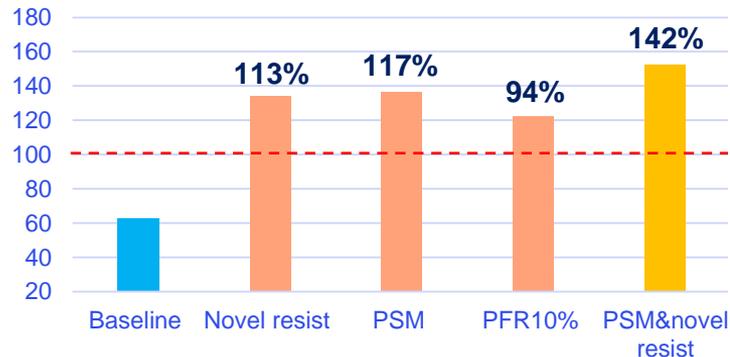
# MO results of RETs for logic Via with min. Pitch=40nm



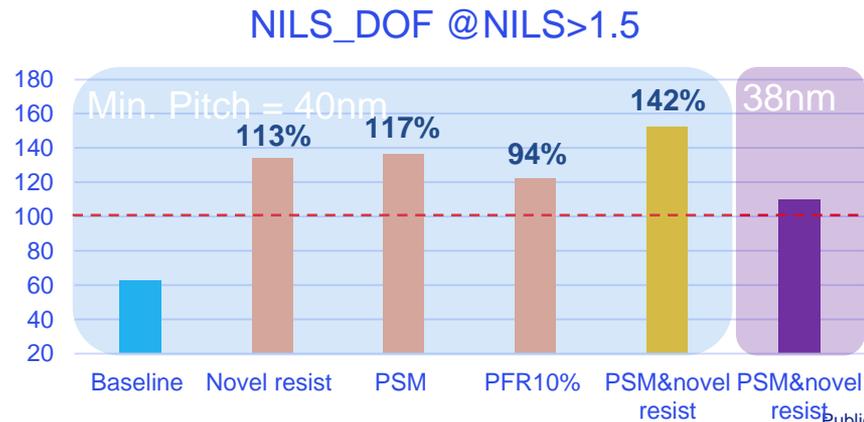
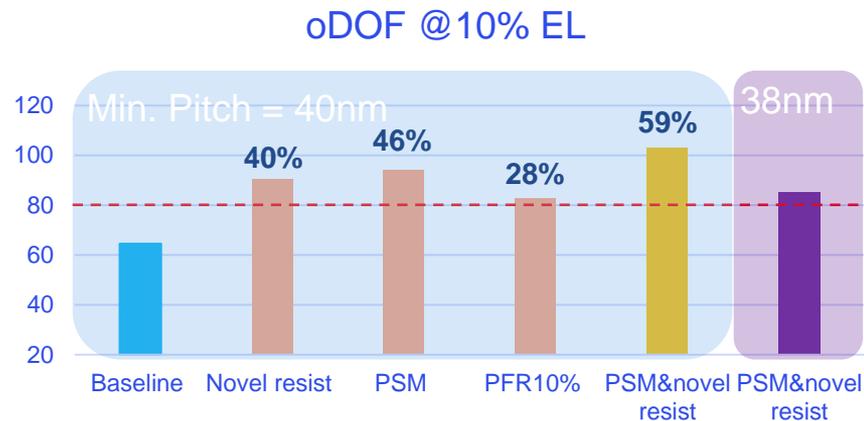
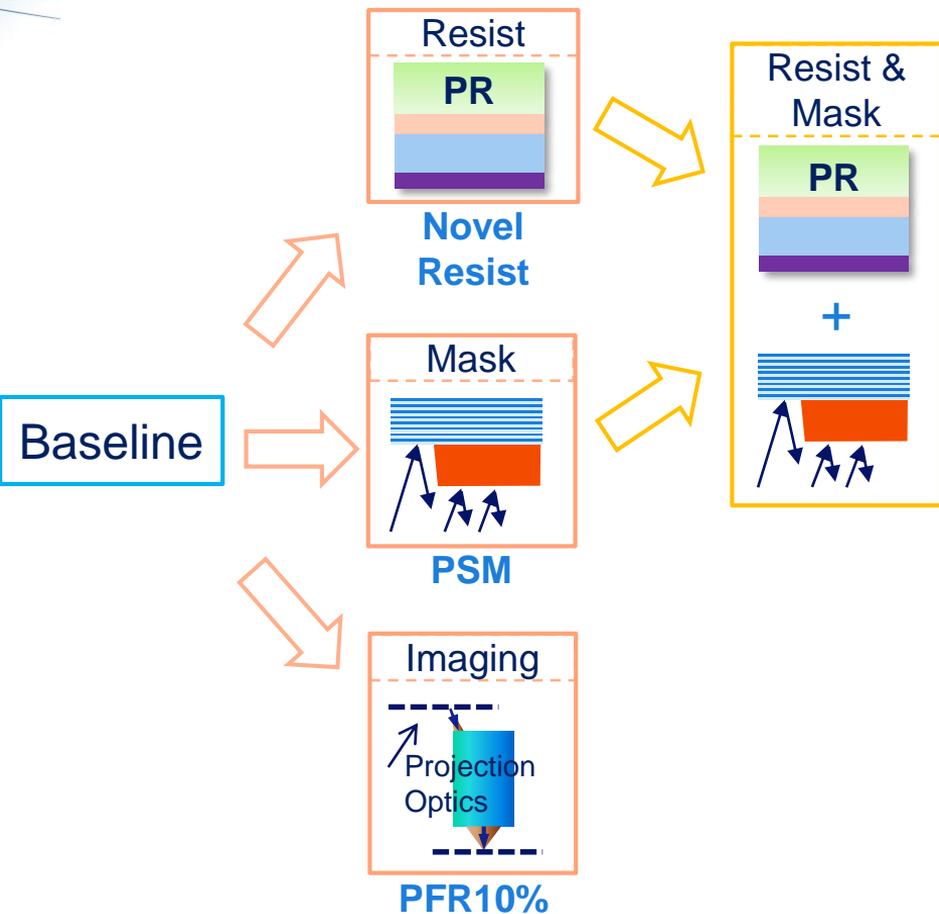
oDOF @10% EL



NILS\_DOE @NILS>1.5



# MO results of RETs for logic Via with min. Pitch=40nm



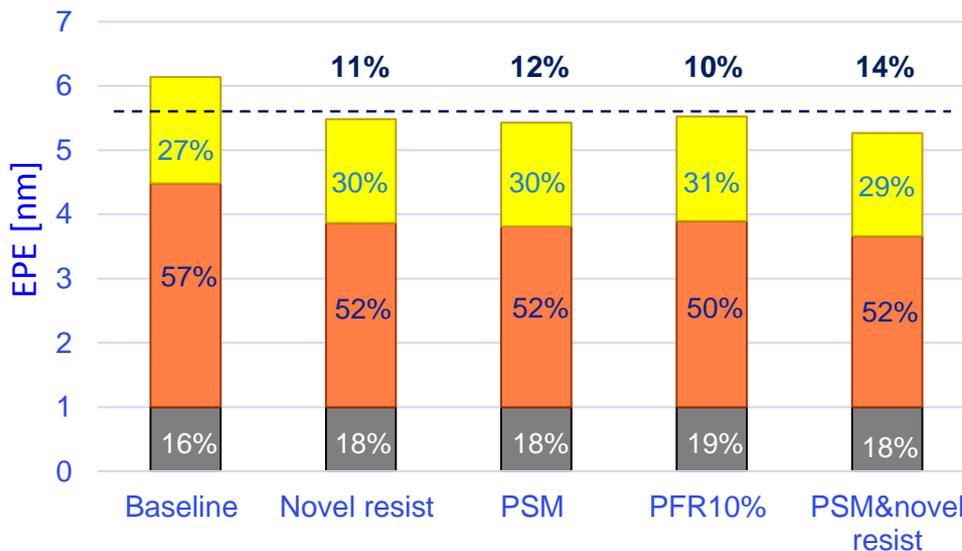
# Assessment of Total Edge Placement Error (EPE)

1. Jan Mulkens et al., SPIE 2017&2018
2. Weimin Gao et. al., SPIE 2020
3. S. G. Hanssen, JM3 17(1), 2018

$$\text{Total EPE} = \text{Systematic} + \text{Local} + \text{Global} =$$

$$\frac{(\text{HR}_{\text{OPC}} + 3\sigma_{\text{PBA}})}{2} + \frac{6\sigma_{\text{LCDU}}}{\sqrt{2}} + \sqrt{(3\sigma_{\text{OVL}})^2 + \left(\frac{3\sigma_{\text{GCDU}}}{2}\right)^2}$$

EPE ~5.6nm was used as spec. <sup>2</sup>



Error budget range  
 Focus error: ±35nm  
 Dose error: ±2%  
 Mask error: ±0.3nm  
 Flare error: 2±0.5%

Global CDU

Local CDU

Systematic

OVL: Overlay  
 PBA: Proximity Bias Average  
 (Scanners CD matching)  
 HR OPC: Half range of optical  
 proximity correction.  
 GCDU: Global CDU  
 LCDU: Local CDU

## Conclusion

- Simulation results show that the current lithographic approach with a standard TaBN absorber does not offer sufficient imaging performance for logic contact patterns of pitch 40nm and below.
- By adopting improved novel resist, PSM or PFR reduction, it can result in a significant increase of oDOF, NILS\_DOE, as well as EPE. These techniques could help to extend the 0.33NA EUV SP to pitch 40nm for logic contact patterns.
- Our investigations indicate that for via pitch smaller than 40nm, a combination of RETs is required. Such low  $k_1$  EUV requires a combination of multiple RETs including not only novel EUV masks but also advanced imaging techniques, enhanced OPC, high-resolution photoresists.

## Future work including investigations of

- SMO/MO with SRAF
- Curvilinear OPC
- Through slit and aberration impact

# Thank You

# ASML

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